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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/711,983	11/14/2000	Robin Harker	COLGRA P21AUS	8740

7590 07/18/2003

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EXAMINER

DAMIANO, ANNE L

ART UNIT

PAPER NUMBER

2184

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	09/711,983	HARKER, ROBIN
	Examiner Anne L Damiano	Art Unit 2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 November 2000.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-12 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 November 2000 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

<ol style="list-style-type: none"> 1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3)<input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u>. 	<ol style="list-style-type: none"> 4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____. 5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6)<input type="checkbox"/> Other: _____.
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DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. The abstract of the disclosure is objected to because the sentence of lines 10-12 is unclear. The examiner believes that the 3rd reference to the power-supply module 2 should be to the processor module 2. Also, lines 10, 11 and 12 refer to the power-supply module as figure component 2 rather than component 19. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, 5-7 and 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Walker (5,848,230).

As in claim 1, Walker discloses a computer system comprising a multiplicity of processors interconnected with one another (figure 1: components 34 and 35), and power-supply means common to all the processors, wherein the power-supply means includes means affording fault-tolerating redundancy (figure 1: components 16, 17 and 18 and column 5: lines 33-34).

As in claim 2, Walker discloses the processors being interconnected for operation in parallel with one another (column 5: lines 63-65). (Multiple CPU's being able to read and write to the disk storage unit implies parallel processing.)

As in claim 5, Walker discloses the power-supply means comprising a plurality of power-supply modules, and means coupling the power-supply modules in parallel with one another for supplying power to the processors (figure 3: components 104, 106 and 108 and column 8: lines 16-20).

As in claim 6, Walker discloses each power-supply module including circuitry responsive to the occurrence of a fault within that respective power-supply module to isolate that individual power-supply module from supplying power to the processors (column 4: lines 62-67 and column 8: lines 21-39).

As in claim 7, Walker discloses the circuitry being diode circuitry (figure 3: components 104, 106 and 108 and column 8: lines 25-29).

As in claim 9, Walker discloses the power-supply means comprising a plurality of pairs of power-supply modules, means coupling the two power-supply modules of each said pair together for supplying power in parallel with one another, and means coupling the pair of power-supply modules in parallel with one another for supplying power to the processors (figure 3: component 104, 106, 108 and column 4: lines 62-67, column 8: lines 4-6). (When one of the power-supplies fails, the remaining power-supply pair supplies power to the processors in parallel.)

As in claim 10, Walker discloses each power-supply module of each pair including circuitry responsive to the occurrence of a fault within that respective power-supply module to isolate that power supply module from supplying power in parallel with the other power-supply module of the respective pair (column 8: lines 6-9 and lines 25-39).

As in claim 11, Walker discloses the circuitry being diode circuitry (figure 3: components 104, 106 and 108 and column 8: lines 25-39).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker as applied to claim 1 above, and further in view of Doustou, III et al. (6,392,872).

Regarding claim 3, Walker discloses the computer system with multiple processors and fault-tolerant power-supply means above. However, Walker does not specifically disclose the means in which his system is physically supported.

Doustou discloses processor modules, cabinet means, means mounting the processor modules side-by-side with one another within the cabinet means, and means mounting the power-supply means within the cabinet means (column 4: lines 12-14, lines 28-30, column 8: lines 62-67 and figure 11: component 165).

It would have been obvious to a person skilled in the art at the time the invention was made to physically support the system taught by Walker, using the housing means taught by Doustou. It would have been obvious because Walker's system inevitably must be housed and Doustou teaches a housing method that decreases over all cost and complexity for systems with multiple power supplies. A person skilled in the art would have understood the desire to minimize cost and complexity in the implementation of Walker's system.

As in claim 4, Doustou discloses the means mounting the processor modules within the cabinet means comprising racking, the racking including tracks, and the processor modules being mounted on the tracks for sliding movement selectively in and out of the cabinet means (column

4: lines 12-16). (Slidably disposed means prepared to slide, which implies some sort of tracks must exist on the racks.)

7. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker as applied to claims 1, 5, 6, 9 and 10 above, and further in view of Lewis et al. (6,289,467).

Regarding claims 8, Walker discloses the power-supply module including circuitry responsive to the occurrence of a fault within that respective power-supply module to isolate that individual power-supply module from supplying power to the processors, above. However, Walker does not specifically disclose the circuitry isolating a power-supply module responsive to reduction in voltage output.

Lewis discloses a voltage sensor that monitors the voltage level of power-supply modules (column 1: lines 44-48) to determine the state of the power-supplies.

It would have been obvious to a person skilled in the art at the time the invention was made to include circuitry for monitoring the power-supply voltage levels as taught by Lewis, in the system taught by Walker. It would have been obvious because Walker teaches isolating a power-supply responsive to a detected fault and Lewis teaches that a low voltage output can cause damage to processor modules (column 1: lines 35-38). A person skilled in the art would have understood that detecting voltage levels for a reduction in voltage output of the power-supply modules would be completed in Walker's system when detecting for a power-supply fault.

Regarding claim 12, Walker discloses the power-supply means including pairs of power-supply modules including circuitry responsive to the occurrence of a fault within that respective power-supply module to isolate that individual power-supply module from supplying power to the processors, above. However, Walker does not specifically disclose the circuitry isolating a power-supply responsive to reduction in voltage output.

Lewis discloses a voltage monitor that monitors the voltage level of power-supply modules (column 1: lines 44-48) to determine the state of the power-supplies.

It would have been obvious to a person skilled in the art at the time the invention was made to include circuitry for monitoring the power-supply voltage levels as taught by Lewis, in the system taught by Walker. It would have been obvious because Walker teaches isolating a power-supply responsive to a detected fault and Lewis teaches that a low voltage output can cause damage to processor modules (column 1: lines 35-38). A person skilled in the art would have understood that detecting voltage levels for a reduction in voltage output of the power-supply modules would be completed in Walker's system when detecting for a power-supply fault.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

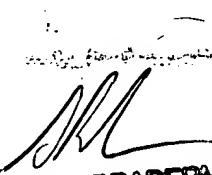
See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9:00AM-6:30PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9731. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ALD
July 10, 2003



SCOTT BADERMAN
PRIMARY EXAMINER